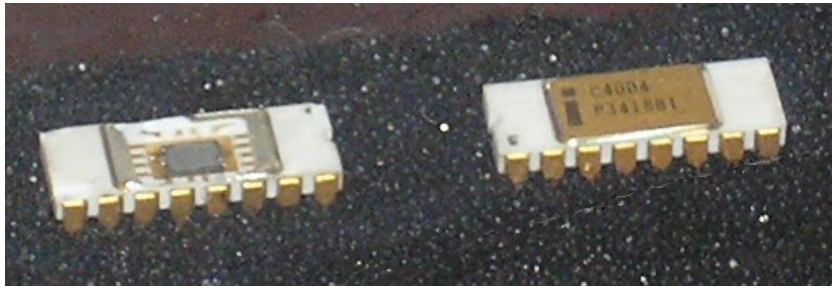
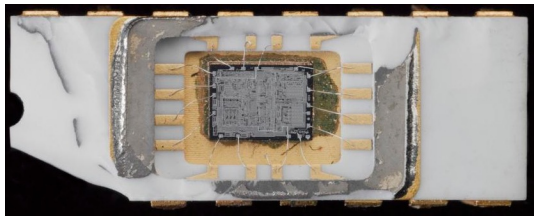
CSCI 210: Computer Architecture
Lecture 25: Data Path 2

Stephen Checkoway

Slides from Cynthia Taylor

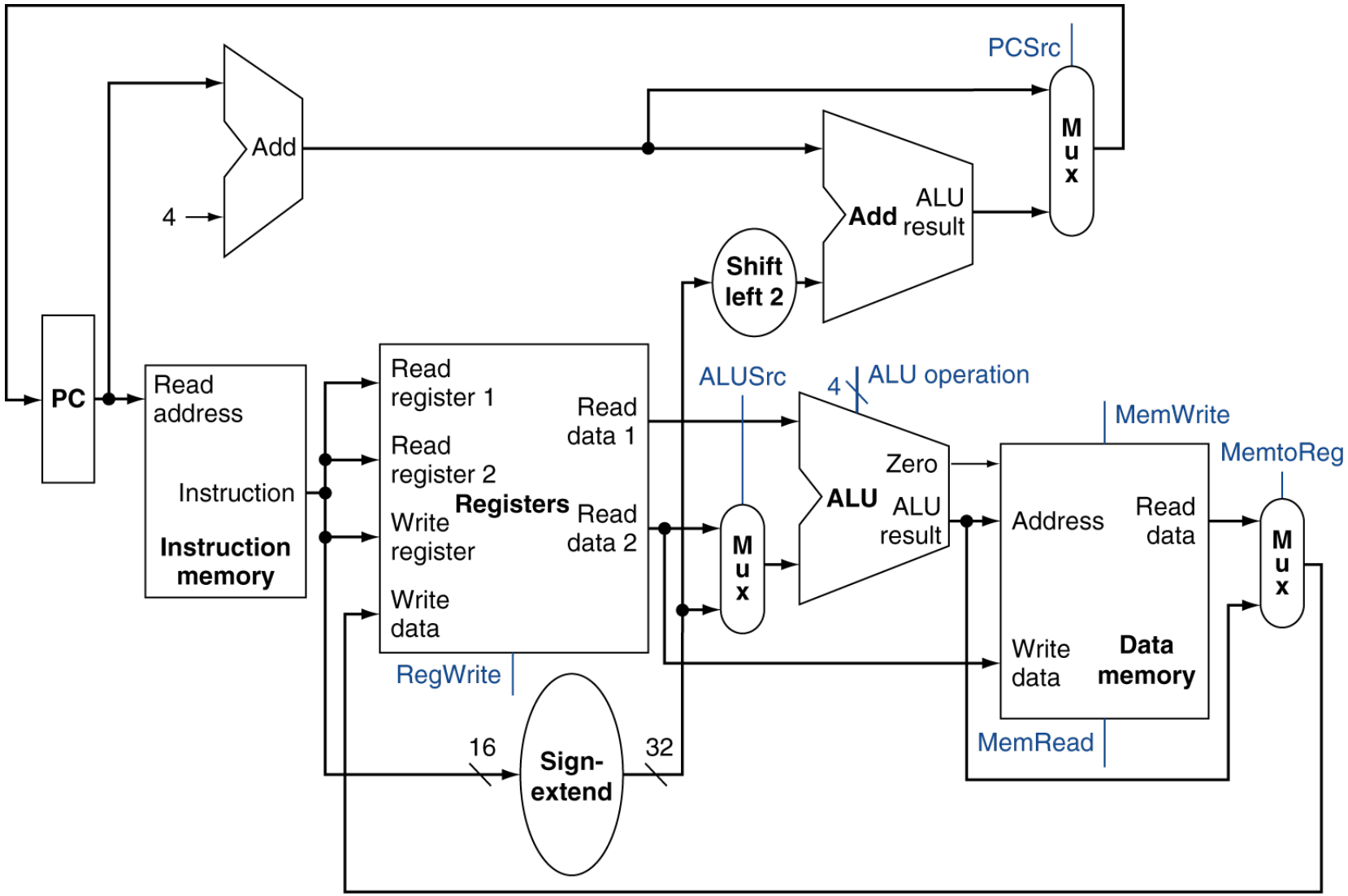
CS History: Intel 4004



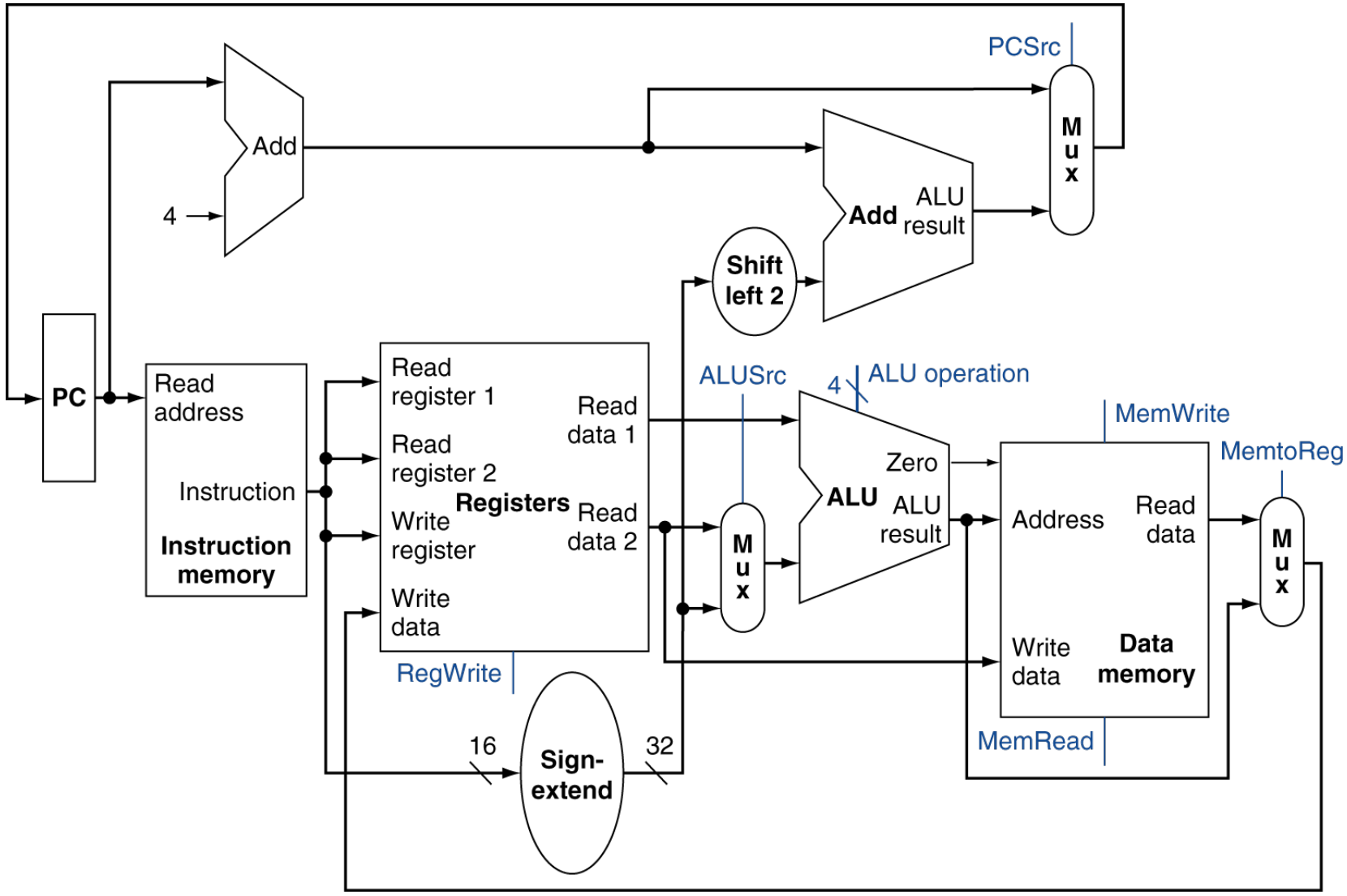


- First commercially available microprocessor (single chip with both data processing logic and control)
- Released in 1971
- Had 12-bit addresses, 8-bit instructions, and 4-bit data words
- 16 4-bit registers
- Designed for Binary-Coded Decimal, in which every decimal digit is stored as a 4-bit value
  - Support for BCD is still present in x86

Datapath (still simplified a bit)



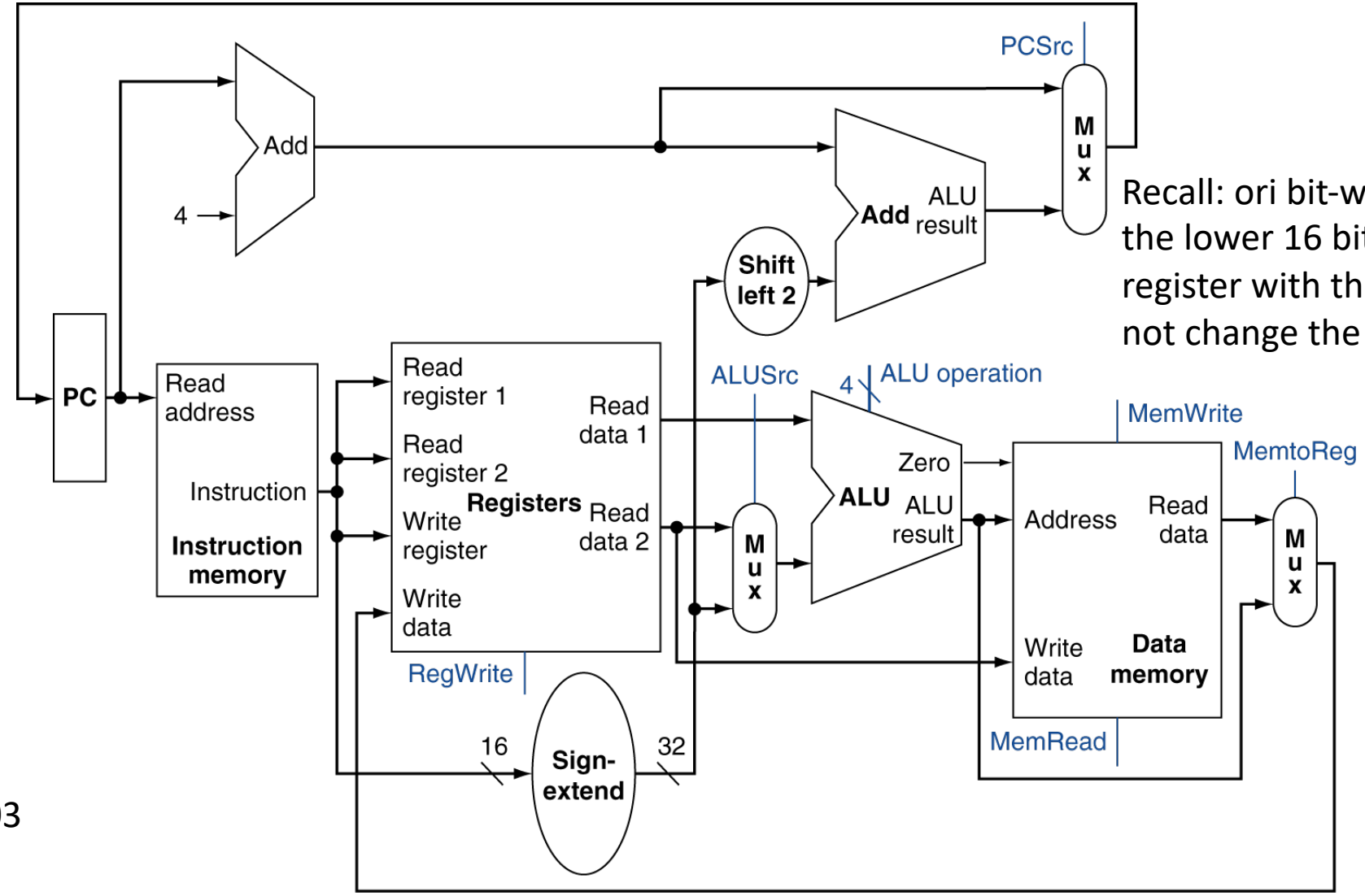
addi $t1, $t0, -1



$t0 holds 10

op = 0x08	rs = 8	rt = 9	imm = 0xFFFF

What do we need to add to support ori?



Recall: ori bit-wise ors the lower 16 bits of the specified register with the immediate. It does not change the upper 16 bits.

ori $t0, $t1, 0x8003
$t1 holds 5

op = 0x0D	rs = 9	rt = 8	imm = 0x8003

Imagine a slightly different architecture with an ori instruction that sign-extends its immediate value. If $t1 has value 5, what value does $t0 have after

```
ori $t0, $t1, 0x8003
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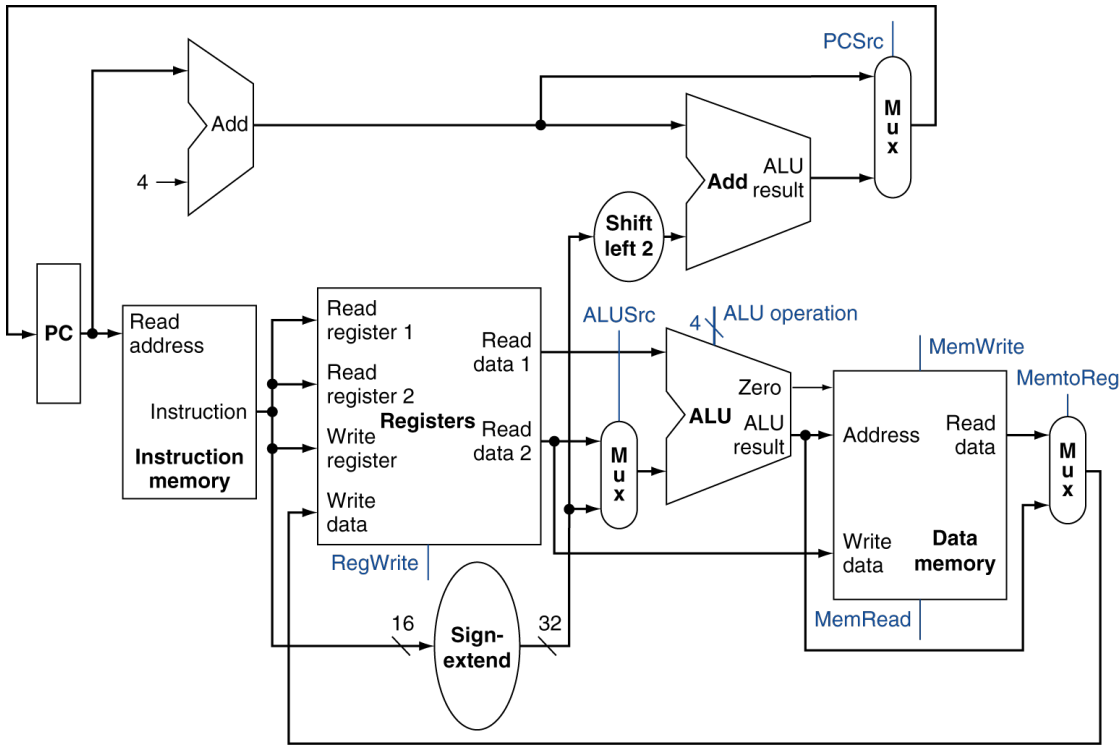
A. 0x00008005

B. 0x00008007

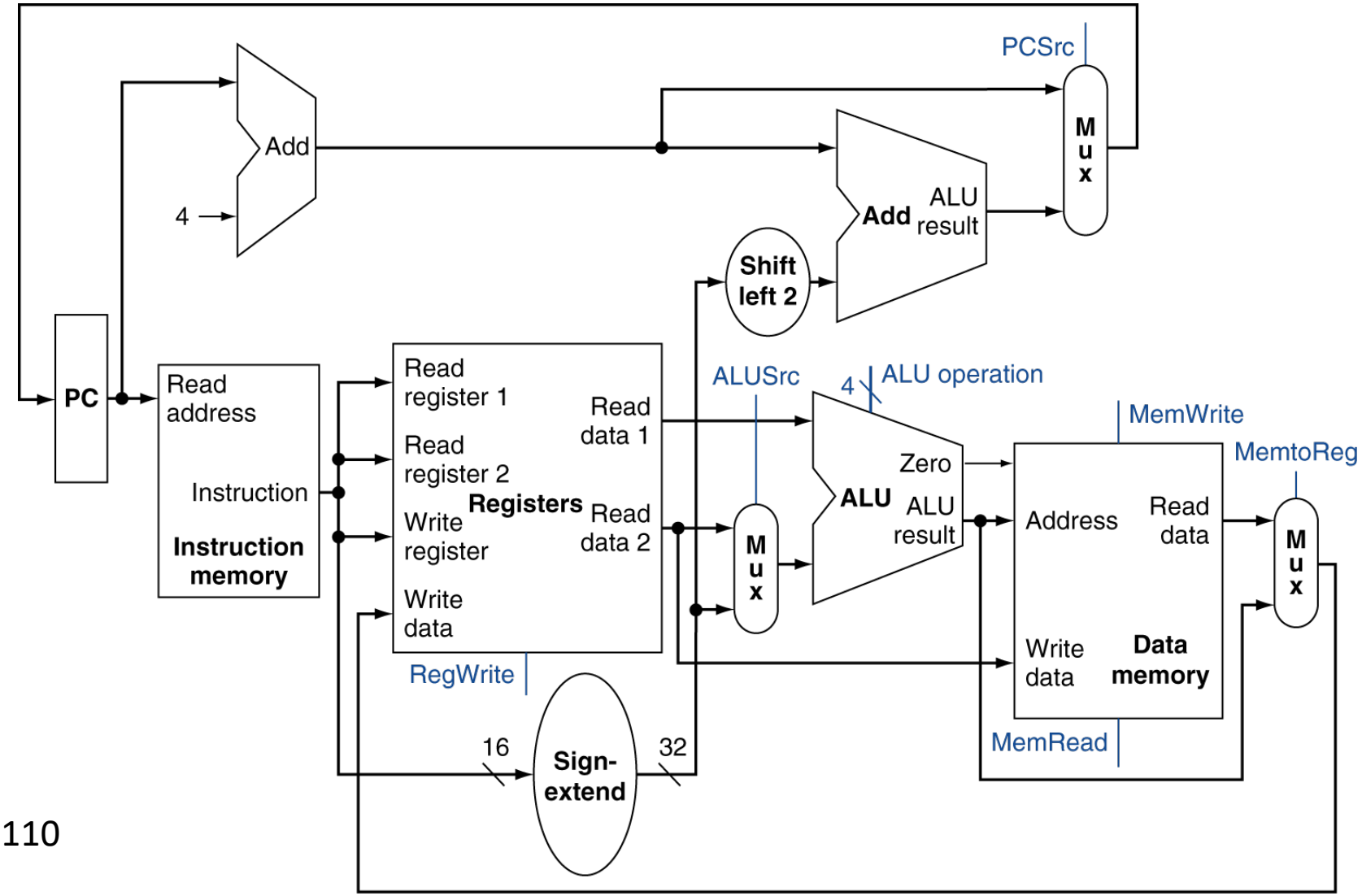
C. 0x88888007

D. 0x80008005

E. 0xFFFF8007



sw $t1, 8($t0)

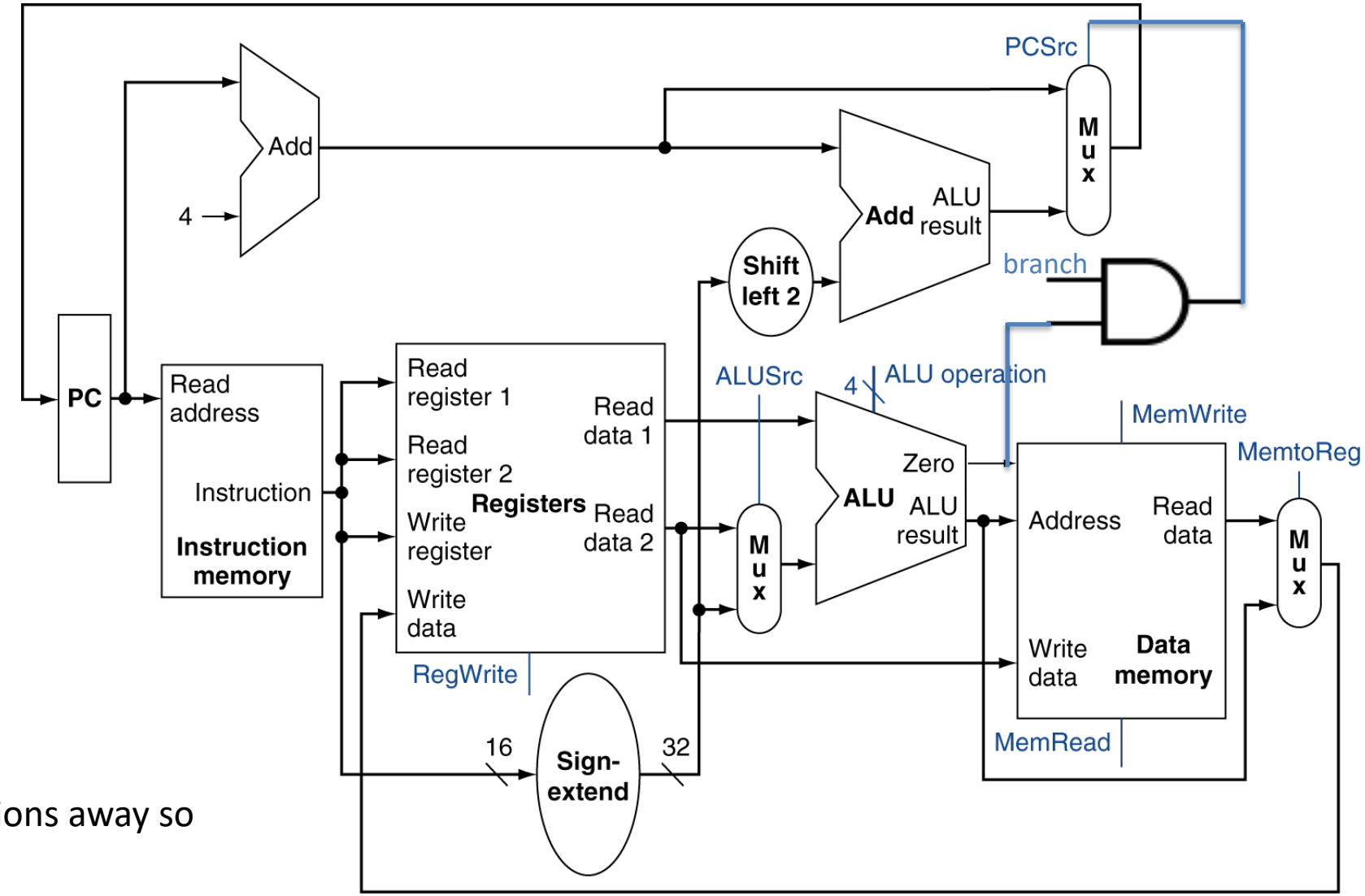


$t0 holds 0x07AB8110

$t1 holds 5

op = 0x2B	rs = 8	rt = 9	imm = 0x0008

beq $s0, $t0, label



$s0 holds 10
$t0 holds 10
label is 33 instructions away so
offset = 0x0020

op = 0x2B	rs = 16	rt = 8	imm = 0x0020

Composing the Elements

- Data path executes one instruction in one clock cycle
  - Each data path element can only do one function at a time
  - Hence, we need separate instruction and data memories, ALU and adders, etc
- Use multiplexers where alternative data sources are used for different instructions
  - Each multiplexer will need select inputs to choose which input to use as the output

Key Points

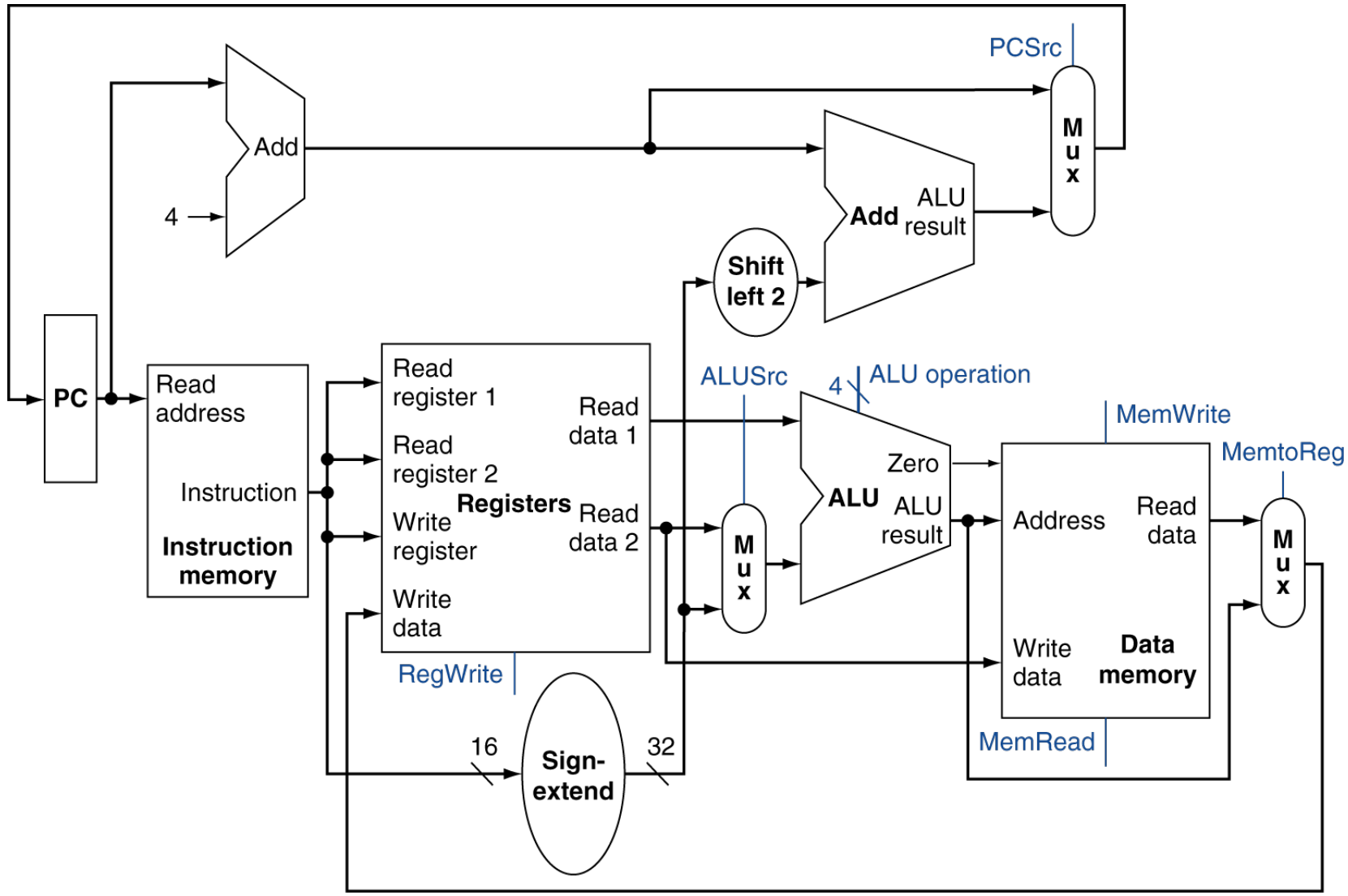
- CPU is just a collection of state and combinational logic
- We just designed a very rich processor, at least in terms of functionality
- ET = IC * CPI * Cycle Time
  - Where cycle time is determined by how much work the processor has to do each clock cycle for one iteration of fetch, decode, execute

What's next?

All of those blue inputs are **control** signals

They control how the data flows through the data path

Each instruction (opcode + funct) determines the control signals



Reading

- Next lecture: Control Path
  - Section 5.4